Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method of programming and erasing an electrically erasable programmable read-only memory (EEPROM) device comprising performing a band-to-band tunneling induced hot-electrons (BTBTIHE) program via a program bit-line (Pb1) and performing a Fowler-Nordheim (FN) tunneling erase via an erase bit-line (Eb1).

[c2] 2.The method of claim 1 wherein the EEPEOM device comprises:

a P-type transistor, a source of the P-type transistor being electrically connected to the program bit-line;

an N-type transistor, a source of the N-type transistor being electrically connected to the erase bit-line; and

a double gate P-type transistor, a drain of the double gate P-type transistor being electrically connected to a drain of the P-type transistor and a drain of the N-type transistor.

[c3] 3.The method of claim 2 wherein both the P-type transistor and the N-type transistor are select gate transistors.

[c4] 4.The method of claim 2 wherein the double gate P-type transistor is an EEPROM cell.

[c5] 5.The method of claim 2 wherein the band-to-band tunneling induced hot-electrons program comprises the following steps:
supplying a first positive potential to a control gate of the double gate P-type transistor;
supplying a first negative potential to a gate of the P-type transistor to turn on the P-type transistor; and
supplying a second negative potential to the program bit-line to pass the second negative potential to the drain of the double gate P-type transistor.

[c6] 6.The method of claim 5 wherein the hot electrons are generated at a junction of the drain of the double gate P-type transistor due to band-to-band tunneling induced electron-hole pair generation.

[c7] 7.The method of claim 2 wherein the Fowler-Nordheim tunneling erase comprises the following steps:
supplying a third negative potential to a control gate of the double gate P-type transistor;
supplying a second positive potential to a gate of the N-type transistor to turn on the N-type transistor; and
supplying a third positive potential to the erase bit-line to pass the third positive potential to the drain of the

double gate P-type transistor.

[c8] 8.The method of claim 7 wherein a potential difference between the control gate of the double gate P-type transistor and the drain of the double gate P-type transistor causes the Fowler-Nordheim tunneling erase.

[c9] 9.The method of claim 2 further comprising a reading method comprising the following steps:
supplying a fourth positive potential to a source line of the double gate P-type transistor; and
supplying a potential lower than the fourth positive potential to the program bit-line.

[c10] 10.An electrically erasable programmable read-only memory (EEPROM) device programmed by a band-to-band tunneling induced hot-electrons (BTBTIHE) program and erased by a Fowler-Nordheim (FN) tunneling erase comprising:
a P-type transistor, a source of the P-type transistor being electrically connected to a program bit-line (Pb1);
an N-type transistor, a source of the N-type transistor being electrically connected to an erase bit-line (Eb1); and
a double gate P-type transistor, a drain of the double gate P-type transistor being electrically connected to a drain of the P-type transistor and a drain of the N-type

transistor.

[c11] 11.TheEEPROM device of claim 10 wherein both the P-type transistor and the N-type transistor are select gate transistors.

[c12] 12.The EEPROM device of claim 10 wherein the double gate P-type transistor is an EEPROM cell.

[c13] 13.The EEPROM device of claim 12 wherein the double gate P-type transistor further comprises a source electrically connected to a source line and a channel between the source and the drain.

[c14] 14.The EEPROM device of claim 13 wherein the double gate P-type transistor further comprises a tunnel oxide layer covering a top surface of the channel, a floating gate disposed on a top surface of the tunnel oxide layer, an isolation layer covering a surface of the floating gate, and a control gate disposed on a top surface of the isolation layer.

[c15] 15.The EEPROM device of claim 14 wherein the band-to-band tunneling induced hot-electrons program comprises the following steps:
supplying a first positive potential to the control gate of the double gate P-type transistor;
supplying a first negative potential to a gate of the P-

type transistor to turn on the P-type transistor; and supplying a negative program potential to the program bit-line to pass the negative program potential to the drain of the double gate P-type transistor.

[c16] 16.The EEPROM device of claim 15 wherein the negative program potential passed to the drain of the double gate P-type transistor through the turned on P-type transistor generates the band-to-band tunneling induced hot electrons at a junction of the drain of the double gate P-type transistor.

[c17] 17.The EEPROM device of claim 14 wherein the Fowler-Nordheim tunneling erase comprises the following steps:
supplying a second negative potential to the control gate of the double gate P-type transistor;
supplying a second positive potential to a gate of the N-type transistor to turn on the N-type transistor; and
supplying a positive erase potential to the erase bit-line to pass the positive erase potential to the drain of the double gate P-type transistor.

[c18] 18.The EEPROM of claim 17 wherein a potential difference between the control gate of the double gate P-type transistor and the drain of the double gate P-type transistor causes the Fowler-Nordheim tunneling erase.

[c19] 19.The EEPROM device of claim 13 further comprising a reading method comprising the following steps:
supplying a third positive potential to the source line of the double gate P-type transistor; and
supplying a potential lower than the third positive potential to the program bit-line.